

BIDIRECTIONAL ESD PROTECTION DIODES

Features

- 495 Watts Peak Pulse Power per Line ($t_p = 8/20\mu s$)
- Protects One Power or I/O Port
- Low Clamping Voltage
- Ultra Low Capacitance: 1.0 pF Typical
- Bidirectional Configuration

Applications

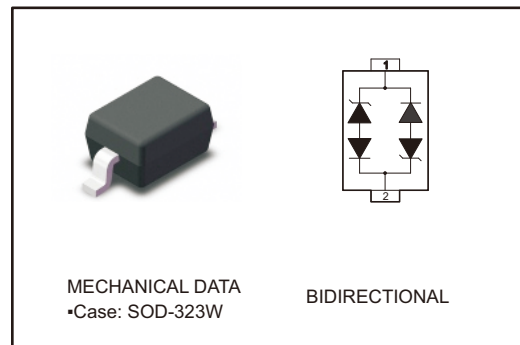
- Ethernet - 10/100/1000 Base T
- Cellular Phones
- Handheld - Wireless Systems
- Personal Digital Assistant(PDA)
- USB Interface

Mechanical Characteristics

- SOD-323W package
- Packaging: Tape and Reel per EIA 481
- Marking : Marking Code
- RoHS Compliant

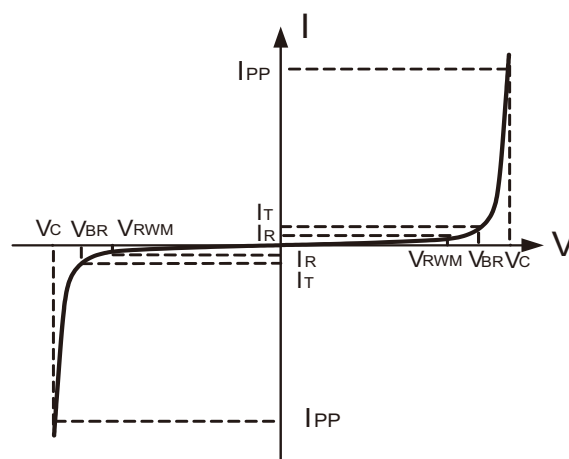
PINNING

PIN	DESCRIPTION
1	Cathode
2	Anode



Electrical Parameters (T=25 °C)

Symbol	Parameter
I_{PP}	Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Reverse Stand- Off Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current





Absolute Ratings

(Tamb=25°C)

Absolute Maximum Rating			
Rating	Symbol	Value	Units
Peak Pulse Power ($t_p = 8/20\mu s$)	P_{PP}	495	W
Peak Pulse Current ($t_p = 8/20\mu s$)	I_{PP}	9	A
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics

Ratings at 25°C ambient temperature unless otherwise specified.

ESDBLC24V0D3						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				24	V
Reverse Breakdown Voltage	V_{BR}	$I_T = 1mA$	26.7		33	V
Reverse Leakage Current	I_R	$V_{RWM} = 24V, T = 25^\circ C$			500	nA
Clamping Voltage	V_C	$I_{PP} = 9A, t_p = 8/20\mu s$		51	55	V
Dynamic Resistance ^{1,2}	R_{DYN}	TLP=0.2/100ns		0.58		Ω
ESD Clamping Voltage ¹	V_C	$I_{PP} = 4A$ $t_p = 0.2/100ns(TLP)$		34.9		V
ESD Clamping Voltage ¹	V_C	$I_{PP} = 16A$ $t_p = 0.2/100ns(TLP)$		41.8		V
Junction Capacitance	C_j	$V_R = 0V, f = 1MHz$		1.0	1.5	pF

Note : 1、 TLP Setting: $t_p = 100ns, t_r = 0.2ns, I_{TLP}$ and V_{TLP} sample window: $t_1 = 70ns$ to $t_2 = 90ns$

2、 Dynamic resistance calculated from $I_{PP} = 4A$ to $I_{PP} = 16A$ using "Best Fit"



Fig.1 Peak Pulse Power vs. Pulse Time

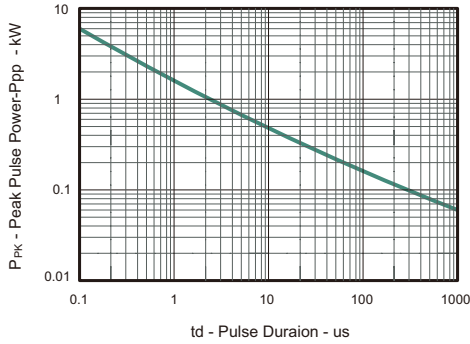


Fig.2 Forward Current Derating Curve

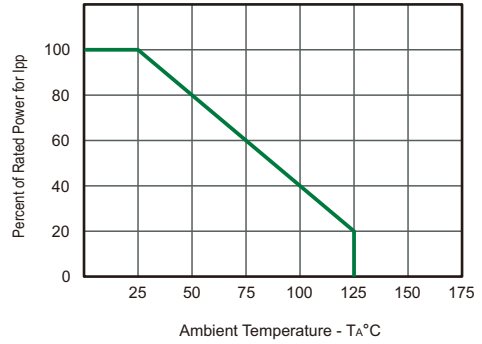


Fig.3 Clamping voltage vs Ipp

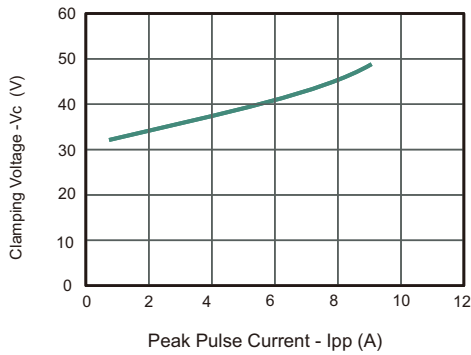


Fig.4 Normalized Junction Capacitance

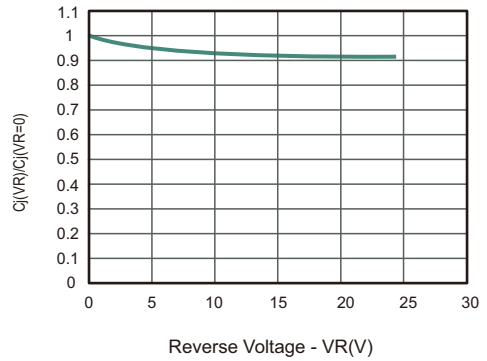


Figure 5: TLP Positive I - V Curve

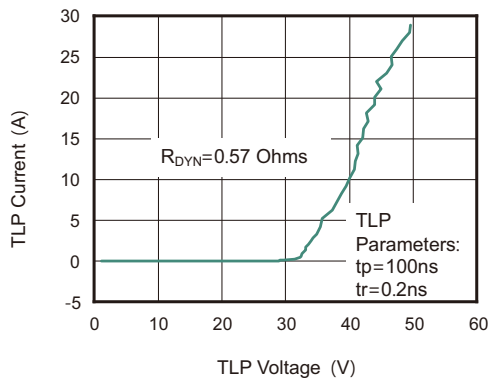
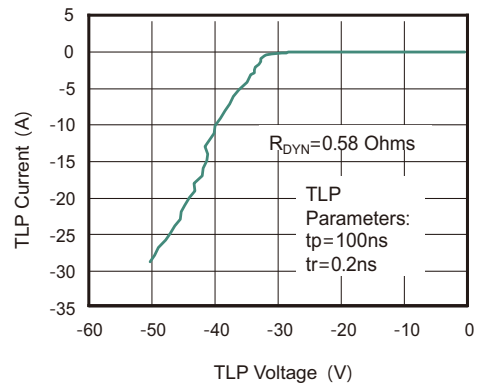


Figure 6: TLP Negative I - V Curve

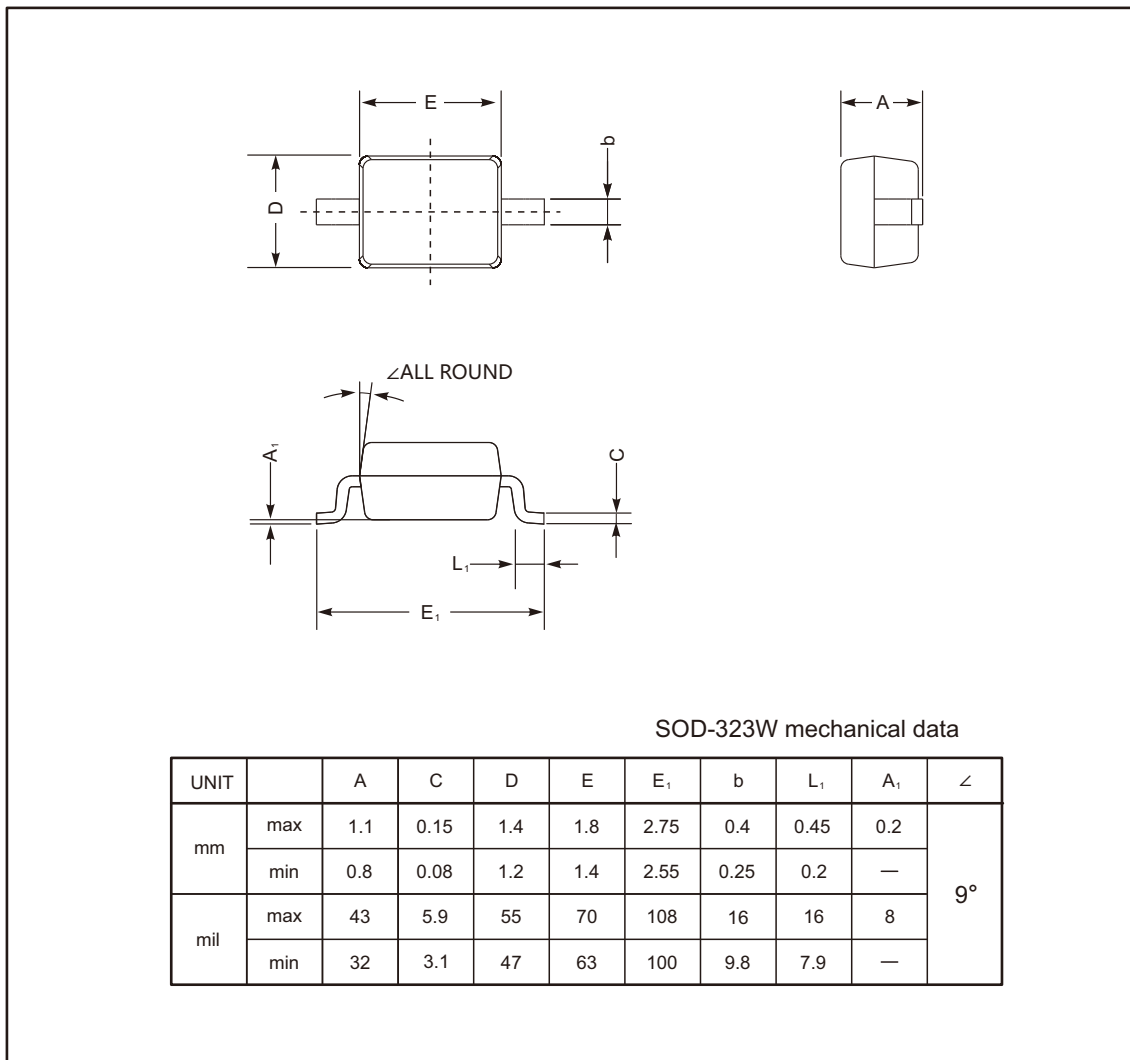




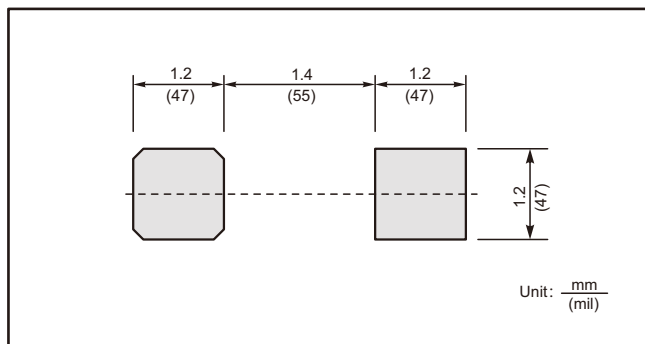
PACKAGE OUTLINE

Plastic surface mounted package; 2 leads

SOD-323W



The recommended mounting pad size



Marking

Type number	Marking code
ESDBLC24V0D3	24L